Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A display driver which drives a plurality of data signal supply lines of an electro-optical device which includes a plurality of pixels, a plurality of scanning lines, a plurality of data lines, the plurality of data signal supply lines, and a plurality of demultiplexers, the plurality of data lines including a plurality of data line groups ~~alternately arranged inward from two opposite sides of the electro-optical device in a shape of comb teeth~~, each of the plurality of data line groups consisting of 3×N numbers of the data lines (N is a natural number), each of the plurality of data signal supply lines transmitting multiplexed data in which N ~~set~~ sets of data signals for first to third color components ~~is~~ are multiplexed, and each of the plurality of demultiplexers demultiplexing the multiplexed data and outputting one of the data signals for the first to third color components to each of the 3×N numbers of data lines, the display driver comprising:

a gray-scale bus to which gray-scale data for one of the first to third color components is supplied~~corresponding to an arrangement order of each of the data lines~~;

N numbers of first data ~~latch~~ latches holding ~~the~~ first gray-scale data ~~on the gray-scale bus based on N clock signal~~ and belonging to one of first to N-th groups, an N-th first data latch holding the first gray-scale data based on an N-th clock signal,

N numbers of second data ~~latch~~ latches holding ~~the~~ second gray-scale data ~~on the gray-scale bus based on N clock signal~~ and belonging to one of the first to N-th groups; an N-th second data latch holding the second gray-scale data based on a 2N-th clock signal,

a multiplexer which generates first multiplexed data in which N set of the first gray-scale data held in the N numbers of first data ~~latch~~ latches is multiplexed and second

multiplexed data in which N ~~set~~ sets of the second gray-scale data held in the N numbers of second data ~~latch is~~ latches are multiplexed; and

a data-signal-supply-line driver circuit in which a plurality of data output sections are ~~disposed corresponding to the arrangement order of each of the data lines,~~ disposed, each of the data output sections outputting a data signal corresponding to the first or second multiplexed data to one of the plurality of data signal supply lines.

2. (Currently Amended) A display driver which drives a plurality of data signal supply lines of an electro-optical device which includes a plurality of pixels, a plurality of scanning lines, a plurality of data lines, the plurality of data signal supply lines, and a plurality of demultiplexers, the plurality of data lines including a plurality of data line groups ~~alternately arranged inward from two opposite sides of the electro-optical device in a shape of comb teeth~~, each of the plurality of data line groups consisting of 3×N numbers of the data lines (N is a natural number), each of the plurality of data signal supply lines transmitting multiplexed data in which N ~~set~~ sets of data signals for first to third color components ~~is~~ are multiplexed, and each of the demultiplexers demultiplexing the multiplexed data and outputting one of the data signals for the first to third color components to each of the 3×N data lines, the display driver comprising:

a gray-scale bus to which gray-scale data for one of the first to third color components is supplied ~~corresponding to an arrangement order of each of the data lines~~;

N numbers of first clock signal ~~line~~ lines being provided with one of 2×N shift clock signals and belonging to one of first to N-th groups;

N numbers of second clock signal ~~line~~ lines being provided with one of the 2×N shift clock signals and belonging to one of the first to N-th groups;

N numbers of first shift ~~register~~ registers including a plurality of flip-flops, shifting a shift start signal in a first shift direction based on one of the 2XN shift clock

signals, outputting a shift output from each of the flip-flops, and belonging to one of the first to N-th groups;

N numbers of second shift ~~register~~ registers including a plurality of flip-flops, shifting the shift start signal in a second shift direction opposite to the first direction based on one of the 2XN shift clock signals, outputting a shift output from each of the flip-flops in ~~the~~ a second shift register, and belonging to one of the first to N-th groups;

N numbers of first data ~~latch~~ latches holding the first gray-scale data ~~on the gray-scale bus based on the shift output from the first shift register~~ and belonging to one of the first to N-th groups, an N-th first data latch holding the first gray-scale data based on an N-th clock signal;

N numbers of second data ~~latch~~ latches holding the second gray-scale data ~~on the gray-scale bus based on the shift output from the second shift register~~ and belonging to one of the first to N-th groups, an N-th second latch holding the second gray-scale data based on an N-th clock signal;

a multiplexer which generates first multiplexed data in which N ~~set~~ sets of the first gray-scale data held in the first data latch ~~is~~ are multiplexed and second multiplexed data in which N ~~set~~ sets of the gray-scale data held in the second data latch ~~is~~ are multiplexed; and

a data-signal-supply-line driver circuit in which a plurality of data output sections are disposed ~~corresponding to the arrangement order of each of the data lines~~, each of the data output sections outputting a data signal corresponding to the first or second multiplexed data to one of the plurality of data signal supply lines,

wherein ~~the~~ a first shift register belonging to a j-th group ($1 \leq j \leq N$, j is an integer) among the first to N-th groups outputs the shift output based on one of the 2XN shift clock signals on ~~the~~ a first clock signal line belonging to the j-th group,

wherein ~~the~~ a second shift register belonging to the j-th group outputs the shift output based on one of the 2XN shift clock signals on ~~the~~ a second clock signal line belonging to the j-th group,

wherein ~~the~~ a first data latch belonging to the j-th group holds the first gray-scale data based on the shift output from the first shift register belonging to the j-th group, and

wherein ~~the~~ a second data latch belonging to the j-th group holds the first gray-scale data based on the shift output from the second shift register belonging to the j-th group.

3. (Currently Amended) The display driver as defined in claim 2, comprising:

a line latch which latches N ~~set~~ sets of the first gray-scale data held in the first data latch and N ~~set~~ sets of the second gray-scale data held in the second data latch,

wherein the multiplexer generates the first multiplexed data in which the N ~~set~~ sets of first gray-scale data from the first data latch among the first gray-scale data held in the line latch is multiplexed, and generates the second multiplexed data in which the N ~~set~~ sets of second gray-scale data from the second data latch among the second gray-scale data held in the line latch ~~is~~ are multiplexed.

4. (Original) The display driver as defined in claim 2, comprising:

a shift clock signal generation circuit which generates the 2×N shift clock signals based on a given reference clock signal,

wherein the gray-scale data is supplied to the gray-scale bus in synchronization with the reference clock signal, and

wherein the 2×N shift clock signals include a period in which the shift clock signals differ in phase.

5. (Original) The display driver as defined in claim 3, comprising:

a shift clock signal generation circuit which generates the 2×N shift clock signals based on a given reference clock signal,

wherein the gray-scale data is supplied to the gray-scale bus in synchronization with the reference clock signal, and

wherein the 2×N shift clock signals include a period in which the shift clock signals differ in phase.

6. (Original) The display driver as defined in claim 4,

wherein the 2×N shift clock signals include a given pulse in a first stage capture period for capturing the shift start signal in each of the first and second shift registers, and differ in phase in a data capture period after the first stage capture period has elapsed.

7. (Original) The display driver as defined in claim 5,

wherein the 2×N shift clock signals include a given pulse in a first stage capture period for capturing the shift start signal in each of the first and second shift registers, and differ in phase in a data capture period after the first stage capture period has elapsed.

8. (Currently Amended) The display driver as defined in claim 4,

wherein N numbers of shift clock ~~signal~~ signals among the 2×N shift clock signals of which phase shift is greater than or equal to 0 and less than π based on the reference clock signal ~~is~~ are supplied to the N numbers of first clock signal ~~line~~lines, and

wherein N numbers of shift clock ~~signal~~ signals among the 2×N shift clock signals of which phase shift is greater than or equal to π and less than 2π based on the reference clock signal ~~is~~ are supplied to the N numbers of second clock signal ~~line~~lines.

9. (Currently Amended) The display driver as defined in claim 5,

wherein N numbers of shift clock ~~signal~~ signals among the 2×N shift clock signals of which phase shift is greater than or equal to 0 and less than π based on the reference clock signal ~~is~~ are supplied to the N numbers of first clock signal ~~line~~lines, and

wherein N numbers of shift clock ~~signal~~ signals among the 2×N shift clock signals of which phase shift is greater than or equal to π and less than 2π based on the reference clock signal ~~is~~ are supplied to the N numbers of second clock signal ~~line~~lines.

10. (Currently Amended) The display driver as defined in claim 6,

wherein N numbers of shift clock ~~signal~~ signals among the 2×N shift clock signals of which phase shift is greater than or equal to 0 and less than π based on the reference clock signal ~~is~~ are supplied to the N numbers of first clock signal ~~line~~lines, and

wherein N numbers of shift clock ~~signal~~ signals among the 2×N shift clock . signals of which phase shift is greater than or equal to π and less than 2π based on the reference clock signal ~~is~~ are supplied to the N numbers of second clock signal ~~line~~lines.

11. (Currently Amended) The display driver as defined in claim 7,

wherein N numbers of shift clock ~~signal~~ signals among the 2×N shift clock signals of which phase shift is greater than or equal to 0 and less than π based on the reference clock signal ~~is~~ are supplied to the N numbers of first clock signal ~~line~~lines, and

wherein N numbers of shift clock ~~signal~~ signals among the 2×N shift clock signals of which phase shift is greater than or equal to π and less than 2π based on the reference clock signal ~~is~~ are supplied to the N numbers of second clock signal ~~line~~lines.

12. (Currently Amended) The display driver as defined in claim 1,

wherein the data-signal-supply-line driver circuit drives the plurality of data signal supply lines from a first side of the electro-optical device based on the first multiplexed data, and drives the plurality of data signal supply lines from a second side of the electro-optical device opposite to the first side based on the second multiplexed data.

13. (Currently Amended) The display driver as defined in claim 2,

wherein the data-signal-supply-line driver circuit drives the plurality of data signal supply lines from a first side of the electro-optical device based on the first multiplexed

data, and drives the plurality of data signal supply lines from a second side of the electro-optical device opposite to the first side based on the second multiplexed data.

14. (Currently Amended) The display driver as defined in claim 3,

wherein the data-signal-supply-line driver circuit drives the plurality of data signal supply lines from a first side of the electro-optical device based on the first multiplexed data, and drives plurality of the data signal supply lines from a second side of the electro-optical device opposite to the first side based on the second multiplexed data.

15. (Currently Amended) The display driver as defined in claim 2,

wherein a direction from a first side to a second side of the electro-optical device in which the plurality of data lines extend is the same as one of the first and second shift directions, the second side being opposite to the first side.

16. (Currently Amended) The display driver as defined in claim 3,

wherein a direction from a first side to a second side of the electro-optical device in which the plurality of data lines extend is the same as one of the first and second shift directions, the second side being opposite to the first side.

17. (Currently Amended) The display driver as defined in claim 1,

wherein, when the ~~scan~~plurality of scanning lines extend in a direction along a long side of the electro-optical device and the plurality of data lines extend in a direction along a short side of the electro-optical device, the display driver is disposed along the short side.

18. (Currently Amended) The display driver as defined in claim 2,

wherein, when the ~~scan~~ plurality of scanning lines extend in a direction along a long side of the electro-optical device and the data lines extend in a direction along a short side of the electro-optical device, the display driver is disposed along the short side.

19. (Currently Amended) The display driver as defined in claim 3,

wherein, when the ~~scan~~ plurality of scanning lines extend in a direction along a long side of the electro-optical device and the data lines extend in a direction along a short side of the electro-optical device, the display driver is disposed along the short side.

20. (Currently Amended) An electro-optical device comprising:

a plurality of pixels;

a plurality of scanning lines;

a plurality of data lines including a plurality of data line groups ~~alternately arranged inward from two opposite sides of the electro-optical device in a shape of comb teeth~~, each of the plurality of data line groups consisting of 3×N numbers of the data lines (N is a natural number);

a plurality of data signal supply lines, each of the plurality of data signal supply lines transmitting multiplexed data in which N ~~set~~ sets of data signals for first to third color components ~~is~~ are multiplexed;

a plurality of demultiplexers, each of the plurality of demultiplexers demultiplexing the multiplexed data and outputting one of the data signals for the first to third color components to each of the 3×N data lines; and

the display driver as defined in claim 1 which drives the data signal supply lines.

21. (Currently Amended) An electro-optical device comprising:

a plurality of pixels;

a plurality of scanning lines;

a plurality of data lines including a plurality of data line groups ~~alternately arranged inward from two opposite sides of the electro-optical device in a shape of comb teeth~~, each of the plurality of data line groups consisting of 3×N numbers of the data lines (N is a natural number);

a plurality of data signal supply lines, each of the plurality of data signal supply lines transmitting multiplexed data in which N ~~set~~ sets of data signals for first to third color components ~~is~~ are multiplexed;

a plurality of demultiplexers, each of the demultiplexers demultiplexing the multiplexed data and outputting one of the data signals for the first to third color components to each of the 3×N data lines; and

the display driver as defined in claim 2 which drives the data signal supply lines.

22. (Currently Amended) An electro-optical device comprising:

a display panel which includes a plurality of pixels, a plurality of scanning lines, a plurality of data lines, ~~the~~ a plurality of data signal supply lines, and a plurality of demultiplexers, the plurality of data lines including a plurality of data line groups ~~alternately arranged inward from two opposite sides of the electro-optical device in a shape of comb teeth~~, each of the plurality of data line groups consisting of 3×N numbers of the data lines (N is a natural number), each of the plurality of data signal supply lines transmitting multiplexed data in which N ~~set~~ sets of data signals for first to third color components ~~is~~ are multiplexed, and each of the plurality of demultiplexers demultiplexing the multiplexed data and outputting one of the data signals for the first to third color components to each of the 3×N numbers of data lines; and

the display driver as defined in claim 1 which drives the data signal supply lines.

23. (Currently Amended) An electro-optical device comprising:

a display panel which includes a plurality of pixels, a plurality of scanning lines, a plurality of data lines, ~~the~~ a plurality of data signal supply lines, and a plurality of demultiplexers, the plurality of data lines including a plurality of data line groups ~~alternately~~

~~arranged inward from two opposite sides of the electro-optical device in a shape of comb teeth~~, each of the plurality of data line groups consisting of 3×N numbers of the data lines (N is a natural number), each of the data signal supply lines transmitting multiplexed data in which N ~~set~~ sets of data signals for first to third color components ~~is~~ are multiplexed, and each of the plurality of demultiplexers demultiplexing the multiplexed data and outputting one of the data signals for the first to third color components to each of the 3×N numbers of data lines; and

the display driver as defined in claim 2 which drives the data signal supply lines.